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REMARKS

Claims 1-26 and 28-40 are all of the claims presently pending in the application.

Entry of this Response is believed proper since no new issues are being presented to the Examiner which would require further consideration and/or search.

Applicants gratefully acknowledge the Examiner's indication that claim 23 is allowed and that claim 36 would be allowable if rewritten in independent form. However, Applicants respectfully submit that all of the claims are allowable.

Claims 1-6, 9-12, 18-22, 24, 25, 30, 34, 35, 37, 39 and 40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Talwar et al. (U.S. Patent No. 6,380,044) (hereinafter "Talwar"). Claims 7-8 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Talwar. Claims 13-17, 26 and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Talwar in view of Yu (U.S. Patent No. 6,235,599). Claims 30 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Talwar in view of Sugawara et al. (U.S. Patent Publication No. 2001/0003364) (hereinafter "Sugawara"). Claim 33 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Talwar in view of Huang et al. (U.S. Patent Publication No. 2004/0159834) (hereinafter "Huang"). Claim 38 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Talwar in view of Feudal et al. (U.S. Patent Publication No. 2004/0126998) (hereinafter "Feudal").

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as defined by claim 1) is directed to a method of forming a semiconductor device. The method includes implanting, on a substrate, a dopant to form a dopant extension region, implanting at least one species, on a substrate, to form a region surrounding at least a portion of the dopant extension region, and annealing the substrate, wherein the at least one species retards a diffusion of the dopant during the annealing of the substrate.

Strained Si complementary metal oxide semiconductor devices, having a strained Si channel on a relaxed Si_{1-x}Ge_x buffer layer offer better device performance over conventional Si CMOS because of the enhancement in both channel electron and hole mobilities, and have been demonstrated for devices as small as about 60nm. For devices smaller than 60nm, an

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extension junction depth of 30nm or below is need. This shallow junction requirement, however, is difficult to achieve for a dopant (e.g., arsenic) junction in N-type metal oxide semiconductor devices in strained Si/Si_{1-x}Ge_x substrates due to significant arsenic-enhanced diffusion (see Application at page 2, lines 8-11).

The claimed invention of exemplary claim 1, on the other hand, provides a method of forming a semiconductor device wherein the at least one species retards a diffusion of the dopant during the annealing of the substrate (e.g., see Application at page 17, lines 10-14). The at least one species implanted on the substrate creates vacancy sinks in the vicinity of the dopant extension region, which thereby retard the diffusion of arsenic (see Application at page 3, lines 16-20).

II. THE PRIOR ART REFERENCES

A. The Talwar Reference

The Examiner alleges that Talwar teaches the claimed invention of claims 1-6, 9-12, 18-22, 24, 25, 30, 34, 35, 37, 39 and 40. Furthermore, the Examiner alleges that the claimed invention of claims 7, 8 and 29 would have been obvious in view of Talwar. Applicants submit, however, that there are elements of the claimed invention, which are neither taught nor suggested by Talwar.

That is, Talwar does not teach or suggest wherein *"said at least one species retarding a diffusion of said dopant during said annealing of said substrate"* as recited in claim 1 and similarly recited in claims 24 and 25.

The Examiner attempts to rely on Figures 1A-1G and columns 7 and 8 of Talwar to support her allegations. The Examiner, however, is clearly incorrect.

That is, nowhere, in these Figures or passages (nor anywhere else for that matter) does Talwar teach or suggest that the at least one species retards a diffusion of the dopant during the annealing of the substrate. Indeed, Talwar merely teaches forming amorphized regions and source /drain regions, which are conventionally formed in most transistors.

Specifically, Talwar merely teaches implanting dopants in amorphized regions (40, 44) to form doped extensions (60, 62). Talwar then teaches forming a source region (80) and a drain region (84) underneath the doped extensions (60, 62), respectively (see Talwar at column 8, lines 34-39). This is a conventionally known method that is used in most transistors. Talwar is actually directed to forming the strippable conformal layer (106) over

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the substrate and the gate to absorb light and to distribute heat to the underlying surfaces.

Talwar does not teach or suggest, however, implanting at least one species wherein the at least one species retards a diffusion of the dopant during the annealing of the substrate. Certain exemplary aspects of the claimed invention provide implanting a dopant (e.g., As in a non-limiting embodiment) to form a dopant extension region (440), implanting a species (e.g., Xe in a non-limiting embodiment) to form a region (430) surrounding the doped extension region and also forming a source region (496) and a drain region (497) (see Application at Figures 4A-4D). An exemplary aspect of the claimed invention recognizes that the at least one species retards a diffusion of the dopant during the annealing of the substrate.

This feature is clearly not taught or suggested by Talwar. In the Office Action, the Examiner attempts to rely on regions (80, 84) of Talwar as allegedly teaching this claimed feature.

However, as pointed out above, these regions (80, 84) are merely source and drain regions (see Talwar at column 8, lines 34-39) and are merely analogous to the source region (496) and the drain region (497) of the claimed invention. The source/drain regions (80, 84) of Talwar merely act as contacts and do not retard a diffusion of the dopant during the annealing of the substrate.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggest by Talwar. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Yu Reference

The Examiner alleges that Yu would have been combined with Talwar to form the claimed invention of claims 13-17, 26 and 28. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions. Specifically, Talwar is directed to a process of fabricating a semiconductor metal-insulator-metal field effect transistor, whereas Yu is directed to a shallow doped junction that is part of an integrated circuit device within a semiconductor substrate. Therefore, these references are

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completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Furthermore, the Examiner's motivation to modify Talwar ("to form a low resistant contact over the source drain region") does not appear to be a problem in Talwar that would require a solution. Talwar already includes a protective layer (106) that is formed over the source and the drain. Thus, as pointed out in MPEP 2143.01, the Examiner's motivation is "improper". That is, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination" (emphasis included in MPEP).

Moreover, neither Talwar nor Yu, nor any combination thereof, teaches or suggests that "*said at least one species retarding a diffusion of said dopant during said annealing of said substrate*" as recited in claim 1 and similarly recited in claims 24 and 25.

The Examiner merely attempts to rely on Yu as allegedly suggesting forming a metal silicide contact over the source and drain region. The Examiner attempts to rely on Figure 1 of Yu to supports her allegations.

Nowhere, however, in this Figure (nor anywhere else for that matter) does Yu teach or suggest that the at least one species retards a diffusion of the dopant during the annealing of the substrate. Thus, Yu fails to make up for the deficiencies of Talwar.

Therefore, Applicants respectfully submit that these references would not have been combined, and that, even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Sugawara Reference

The Examiner alleges that Sugawara would have been combined with Talwar to form the claimed invention of claims 30 and 32. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions. Specifically, Talwar is directed to a process of fabricating a semiconductor metal-insulator-metal field effect transistor, whereas Sugawara is directed to a semiconductor device that is

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capable of increasing the operation speed and reducing the power consumption by providing an nMOS in which the mobility of electrons is increased by a strain effect and a pMOS in which the mobility of positive holes is increased by the strain effect on a common substrate. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Furthermore, the Examiner's motivation to modify Talwar ("to increase mobility of ions so that the speed and the device performance can be increased") does not appear to be a problem in Talwar that would require a solution. Thus, as pointed out in MPEP 2143.01, the Examiner's motivation is "improper". That is, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination" (emphasis included in MPEP).

Moreover, neither Talwar nor Sugawara, nor any combination thereof, teaches or suggests that "*said at least one species retarding a diffusion of said dopant during said annealing of said substrate*" as recited in claim 1 and similarly recited in claims 24 and 25.

The Examiner merely attempts to rely on Sugawara as allegedly suggesting strained and relaxed SiGe substrates that include one of compressive and tensile strain. The Examiner attempts to rely on paragraph [0013] of Sugawara to support her allegations.

Nowhere, however, in this passage (nor anywhere else for that matter) does Sugawara teach or suggest that the at least one species retards a diffusion of the dopant during the annealing of the substrate. Thus, Sugawara fails to make up for the deficiencies of Talwar.

Therefore, Applicants respectfully submit that these references would not have been combined, and that, even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

D. The Huang Reference

The Examiner alleges that Huang would have been combined with Talwar to form the claimed invention of claim 33. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

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Specifically, Talwar is directed to a process of fabricating a semiconductor metal-insulator-metal field effect transistor, whereas Huang is directed to providing a strained silicon layer structure having an enhanced fabrication efficiency for use within a semiconductor product. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Furthermore, the Examiner's motivation to modify Talwar ("to increase the performance of the device as a result of enhanced carrier mobility") does not appear to be a problem in Talwar that would require a solution. Thus, the Examiner's urged combination is based solely on impermissible hindsight.

Moreover, neither Talwar nor Huang, nor any combination thereof, teaches or suggests that "*said at least one species retarding a diffusion of said dopant during said annealing of said substrate*" as recited in claim 1 and similarly recited in claims 24 and 25.

The Examiner merely attempts to rely on Huang as allegedly teaching a device having a strained silicon substrate. The Examiner attempts to rely on paragraphs [0004] through [0019] of Huang to support her allegations.

Nowhere, however, in this passage (nor anywhere else for that matter) does Huang teach or suggest that the at least one species retards a diffusion of the dopant during the annealing of the substrate. Thus, Huang fails to make up for the deficiencies of Talwar.

Therefore, Applicants respectfully submit that these references would not have been combined, and that, even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

E. The Feudal Reference

The Examiner alleges that Feudal would have been combined with Talwar to form the claimed invention of claim 38. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions. Specifically, Talwar is directed to a process of fabricating a semiconductor metal-insulator-metal field effect transistor, whereas Feudal is directed improving the mobility in the channel

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region of a field effect transistor, which improves the switching speed of the transistor.

Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Moreover, neither Talwar nor Feudal, nor any combination thereof, teaches or suggests that “*said at least one species retarding a diffusion of said dopant during said annealing of said substrate*” as recited in claim 1 and similarly recited in claims 24 and 25.

The Examiner merely attempts to rely on Feudal as allegedly suggesting forming a strained channel region. The Examiner attempts to rely on paragraphs [0020] through [0022] of Feudal to supports her allegations.

Nowhere, however, in this passage (nor anywhere else for that matter) does Feudal teach or suggest that the at least one species retards a diffusion of the dopant during the annealing of the substrate. Thus, Feudal fails to make up for the deficiencies of Talwar.

Therefore, Applicants respectfully submit that these references would not have been combined, and that, even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In response to the Examiner’s objection to the claim, Applicants respectfully disagree with the Examiners’ objection. That is, Applicants submit that “comprises at least one of” is proper claim language for claiming a list of elements. Applicants respectfully request the Examiner to withdraw this objection.

In response to the Examiner’s objection to the Specification, Applicants again respectfully submit that the subject matter of claim 23 has proper antecedent basis in the Specification.

Specifically, the Specification recites “It is noted that, after step 510 (e.g., performing the atom/ion species implantation) and before step 520 of forming the As extension implant, an anneal could be optionally performed immediately thereafter to remove the damage created by the species implantation” (see Application at page 20, line 21 through page 21, line 1). The Examiner is respectfully requested to withdraw this objection.

Additionally, if the Examiner is not persuaded by Applicants’ remarks above, Applicants respectfully request the Examiner to respond to Applicants’ remarks, as opposed to

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merely repeating the Examiner's objection from the previous Office Action.

In view of the foregoing, Applicants submit that claims 1-26 and 28-40, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Date: March 11, 2005

Respectfully Submitted,



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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Response Under 37 CFR §1.116 by facsimile with the United States Patent and Trademark Office to Examiner Brook Kebede, Group Art Unit 2823 at fax number (703) 872-9306 this 11th day of March, 2005.



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